Growth of High-Quality Graphene on Single-Crystalline SiC Thin Film on Affordable Wafers for Beyond 5G Devices

Graphene is a promising material for beyond 5G devices due to its low environmental load. However, one of the primary challenges in realizing such devices is the scalable growth of high-quality graphene on device-type wafers; it is difficult to do so while balancing both quality and affordability. We propose a new method for growing high-quality graphene on a new template named "hybrid SiC." The quality of graphene on this hybrid SiC is comparable to that on SiC bulk crystals. Graphene on the hybrid SiC exhibited high carrier mobilities, and transistors using the graphene showed the potential to operate at terahertz frequencies.

Graphene, which is a two-dimensional honeycomb lattice of carbon atoms, exhibits excellent electronic properties, such as an extremely high carrier mobility, and inhibits short-channel effects. These properties make graphene attractive for use beyond 5G devices. In order to realize graphene-based devices, it is essential to develop methods for the scalable growth of high-quality graphene on semi-insulating device-type wafers. One promising method involves growing graphene on SiC bulk single crystals by annealing the crystals to sublimate the surface Si atoms. Unfortunately, however, the price of semi-insulating SiC bulk crystals is high, making it difficult to balance affordability and quality when using graphene.

To achieve such a balance, we present a new method for growing high-quality few-layer graphene (FLG) using a new template, called "hybrid SiC," which consists of a high-quality SiC thin film, by peeling from a SiC bulk crystal, and an affordable device-type wafer [1].

The growth method is shown schematically in Fig. 1.

The growth process is classified into two parts. The first part is the fabrication of the hybrid SiC. First, H^+ ions are implanted in the Si face of an on-axis 3-inch SiC bulk crystal to form a cut line, at which the SiC crystal can be separated easily. Then, the SiC bulk crystal is bonded to a device-type wafer (a 3-inch poly-SiC wafer was used in this study) with an intermediate layer. During the bonding, pressure is applied by the wafer's own weight and heating at ~600 K is performed. This is followed by peeling the SiC bulk crystal from the device-type wafer. The device-type wafer can be, for example, poly-SiC, Si, and sapphire. Finally, the surface is atomically flattened by chemomechanical polishing (CMP). The quality of the hybrid SiC was shown to be comparable to that of bulk SiC crystals by X-ray diffraction and atomic force microscope measurements. This SiC fabrication process is repeatable; namely, multiple hybrid SiCs can be produced by using a SiC bulk crystal. The graphitization was done by using a radio-frequency induction heating furnace installed in a super-clean room.

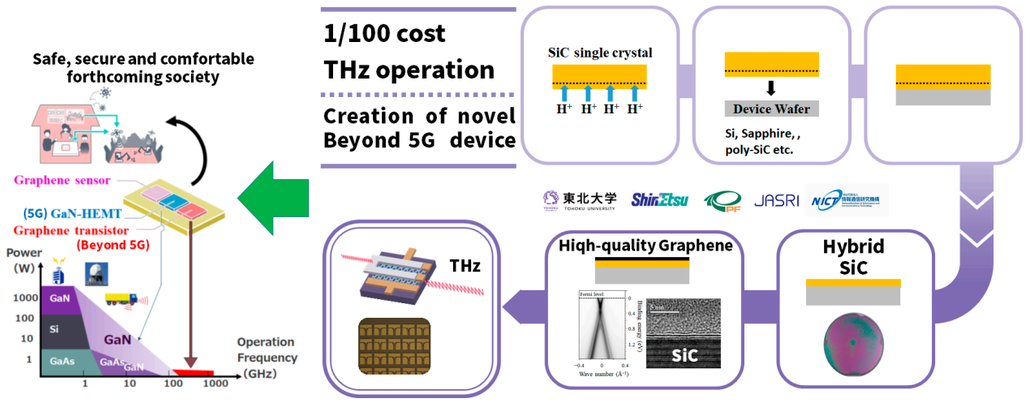

Figure 1: Schematic of our work using the hybrid SiC.

The high-quality FLG grown on the hybrid SiC promises linear band dispersion. To confirm whether this was indeed the case, we recorded the ARPES spectra of the FLG sample on the Si-face and C-face hybrid SiC using vacuum ultraviolet (VUV) radiation at beamline BL-2 MUSASHI [1]. On the Si-face hybrid SiC, the bands were energetically split due to Bernal stacking, and graphene grown on the Si-face SiC bulk crystal was observed. On the other hand, on the C-face hybrid SiC, the bands were not energetically split, but multiple bands appeared at different wave vectors, due to non-Bernal stacking. This difference arises from the absence of the buffer layer between graphene and the C-face hybrid SiC, which works as the template of Bernal stacking. Furthermore, we performed Hall-effect measurements and demonstrated that the carrier mobilities of graphene on the hybrid SiC are high [1].

Finally, we fabricated transistors using graphene on the hybrid SiC. By precisely controlling the surfaces and interfaces surrounding graphene, we simultaneously achieved both complete drain current saturation and large transconductance, which are indispensable for operating at high frequencies. In fact, it was demonstrated by estimating from the DC characteristics that the transistors can operate at THz (10^3 GHz) with a conventional gate length of 100 nm [1].

In summary, we established a method of growing high-quality graphene on device-type wafers, such as poly-SiC, Si, and sapphire at an affordable cost, <1/100 of that using bulk SiC crystals [1]. By using graphene, we can realize THz transistors with a low environmental load. Our work paves the way for next-generation wireless communication systems that will be the basic infrastructure of the forthcoming smart societies. Our work may also enable the monolithic integration of beyond 5G graphene-based devices and existing electronics, such as GaN-based high electron mobility transistors (GaN-HEMTs) for 5G, which use SiC as substrates, owing to the degree of freedom regarding the choice of wafer.

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